Amendments to the Claims:

The Listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A ferroelectric capacitor comprising:

a support insulating film on an integrated circuit substrate and having a trench therein;

a lower electrode on sidewalls and a bottom surface of the trench;

a seed conductive film covering the lower electrode;

a ferroelectric film on the support insulating film and the seed conductive film; and

an upper electrode on the ferroelectric film.

2. (Original) The ferroelectric capacitor of Claim 1 wherein the lower electrode fills the trench and wherein the ferroelectric film extends over all of the seed conductive film and the support insulating film adjacent the seed conductive film.

3. (Original) The ferroelectric capacitor of Claim 1 wherein the lower electrode includes an upper portion thereof extending from the trench to a height relative to the integrated circuit substrate greater than a height of the support insulating film and wherein the seed conductive film covers the upper portion of the lower electrode extending from the trench.

4. (Original) The ferroelectric capacitor of Claim 1, further comprising:

an insulating film between the support insulating film and the substrate; and

a contact plug extending through the insulating film and electrically connecting the lower electrode to an active region of the integrated circuit substrate.

5. (Original) The ferroelectric capacitor of Claim 3 wherein the support insulating film comprises titanium oxide.

6. (Original) The ferroelectric capacitor of Claim 1 wherein the seed conductive film comprises platinum and wherein the ferroelectric film comprises $SrTiO_3$, $BaTiO_3$, $(Ba,Sr)TiO_3$, $Pb(Zr,Ti)O_3$, $SrBi_2Ta_2O_9$, $(Pb,La)(Zr,Ti)O_3$ and/or $Bi_4Ti_3O_{12}$.

7. (Original) The ferroelectric capacitor of Claim 1 wherein the lower electrode comprises a multilayer structure including a lower noble metal layer and an upper noble metal layer with a conductive oxide layer of the lower noble metal therebetween and wherein the lower noble metal layer and the conductive oxide layer are conformal to the sidewalls and the bottom surface of the trench and the upper noble metal layer fills portions of the trench not filled by the lower noble metal layer and the conductive oxide layer.

8. (Original) The ferroelectric capacitor of Claim 7 wherein the seed conductive film comprises platinum.

9. (Original) The ferroelectric capacitor of Claim 7 wherein the upper noble metal layer and the lower noble metal layer comprise platinum, ruthenium, iridium, rhodium, osmium and/or palladium and wherein the conductive oxide layer comprises ruthenium dioxide and/or iridium dioxide.

10. (Original) The ferroelectric capacitor of Claim 1 wherein the lower electrode and the upper electrode comprise a noble metal and/or an oxide thereof.

11. (Original) The ferroelectric capacitor of Claim 10 wherein the noble metal comprises platinum, ruthenium, iridium, rhodium, osmium and/or palladium.

12. (Original) An integrated circuit memory device having a plurality of cells arranged in a cell array, ones of the cells including the ferroelectric capacitor of Claim 1.

13-33. (Canceled).